REMARKS

By this amendment Applicant cancels claim 5 thus claims 1, 3-4, 6-10, 12 and 16-21 are all the claims pending in the present application. All claims stand rejected. Reconsideration and allowance of all pending claims are respectfully requested in view of the following remarks.

ENTRY OF AMENDMENT.

Applicant believes the foregoing amendments should be entered under 37 C.F.R. 1.116 as they do not present any new issues for consideration and/or require additional search. Applicant merely includes the limitations of former claim 5 into claim 1. Since these limitation were already present in the pending claims, additional consideration and/or search is not required. Further the literal scope of the original claims is not narrowed by the foregoing amendments since the newly added limitations were expressly included in the scope of the originally filed claims.

CLAIM REJECTIONS.

35 U.S.C. § 102

1. Claim 1 is rejected under 35 U.S.C. § 102(b) as being anticipated by newly cited U.S. Patent 5,140,681 to Uchiyama et al. Applicant respectfully traverses these rejections for the following reasons.

The Office Action alleges that Uchiyama discloses all the features recited in claim 1. As amended claim 1 recites the feature that *the memory array is further adapted to dynamically alter a size of the first portion and the second portion of the memory array depending on an operational load of the first processor or the second processor.* This claimed feature is not taught or suggested by Uchiyama and thus claim 1 is patentable over Uchiyama. In fact,

Uchiyama teaches away from this limitation by disclosing preset address tables for accessing subdivisions of main memory 5 using predetermined address ranges (col. 5, ll. 15-51). In view of this reconsideration and withdrawal of this rejection is respectfully requested.

2. Claims 10, 12, 16 and 20-21 are rejected under 35 U.S.C. § 102(b) as being anticipated by U.S. Patent 5,636,361 to Ingerman. Applicant respectfully traverses this rejection for the following reasons.

Ingerman discloses a multi-processor system having dual memory subsystems. Ingerman discloses two processors 32, 50 and two bus/memory subsystem groups arranged so that each processor 32, 50 is connected with each bus to access memory subsystems via the associated bus. (Col. 6, ll. 27-34). In the embodiment shown in Fig. 2 (referenced by the Office Action) each separate processor 32, 33 accesses separate memory subsystems 42 and 48 via respective bus lines 40, 46 and caches 34, 52. The Office Action alleges cache memories 34 and 52 and subsystem memories 42 and 48 are analogous to a memory array having first and second portions claimed in claims 10, 12, 16 and 20-21. Applicant respectfully disagrees. It is evident to the skilled artisan that memories 34, 42, 52, 48 referenced in Fig. 2 are separate memory devices as opposed to a memory array having first and second dedicated portions respectively accessible by first and second processors via first and second busses as recited in claim 10. Furthermore, claim 10 recites that the second portion of the memory array is accessible only by the second processor and the first portion accessible only by the first processor. By way of contrast, Ingerman Fig. 2 shows both processors 32, 50 accessing both memory subsystems 42, 48.

In fact, Ingerman expressly teaches away from Applicant's claimed invention by disclosing that two separate memories 42 and 48 are mutually accessed by each processor 34, 52. (and/or each processor 32, 50 has a dedicated cache). This is contrary to Applicant's invention which reduces size, complexity and cost of a multiprocessor system by sharing memory between two or more processors (see for example, specification pg. 2, ll. 16-18). For the foregoing

reasons, Ingerman cannot anticipate or render obvious Applicant's claims and Applicant respectfully requests reconsideration and withdrawal of this rejection.

35 U.S.C. § 103

Applicants claims 1, 3-9 and 18-19 are further rejected under 35 U.S.C. § 103(a) as being unpatentable over Uchiyama and/or Ingerman in further view of previously cited U.S. Patent Application 2002/0184445) to Cherabuddi. Applicant traverses these rejections for the following reasons.

None of the cited references teaches or suggests the claimed limitation of *the memory array is further adapted to dynamically alter a size of the first portion and the second portion of the memory array depending on an operational load of the first processor or the second processor.* The Office Action alleges this is disclosed by Cherabuddi at par. [0025]. Applicant respectfully disagrees. While Cherabuddi does mention dynamically allocating resources of cache memory 23 in response to needs of the CPUs, Cherabuddi does not teach or suggest altering the size of the first portion and second portion which still maintain exclusivity for access by respective first and second processors.

NOT NECESSARY

Instead, Cherabuddi is referencing the ability to alternate partitioning of a single cache memory between two modes as discussed in par. [0009-0011]. For example, in the two-thread mode (both processors are active), each processor uses a corresponding dedicated portion of the cache memory (i.e., sharing the cache). In a one-thread mode (only one processor is active), the cache can be entirely allocated such that the active processor can use the entire cache including both memory partitions. This means that in a one-thread mode, the alleged second memory partition may be accessible by the first processor.

By way of contrast, Applicant's claim 1 recites first and second portions for exclusive access by respective processors while varying the size of the first and second portions depending on the respective processor load. Since Cherabuddi, Uchiyama and/or Ingerman, taken alone or in combination fail to teach or suggest this claimed feature, Applicant's claims are patentable

over the cited art. In view of the foregoing, reconsideration and withdrawal of all §103 rejections are respectfully requested.

CONCLUSION.

In view of the above, reconsideration and allowance of this application are now believed to be in order, and such actions are hereby solicited. If any points remain in issue which the Examiner feels may be best resolved through a personal or telephone interview, the Examiner is kindly requested to contact the undersigned at the telephone number listed below. Applicant hereby petitions for any extension of time which may be required to maintain the pendency of this case, and any required fee or deficiency thereof, except for the Issue Fee, is to be charged to **Deposit Account # 50-0221.**

Respectfully submitted,

Stuart A. Whittington
Registration No. 45,215
Intel Corporation
(480) 554-2895

c/o
Blakely, Sokoloff, Taylor & Zafman, LLP
12400 Wilshire Blvd., Seventh Floor
Los Angeles, CA. 90025-1026
(503) 264-0967

Date: 3/31/04